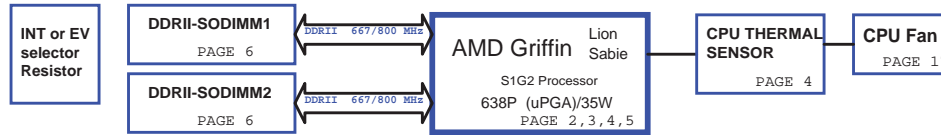


# ZY5/ZY5D SYSTEM BLOCK DIAGRAM



CPU CORE ISL6265A	PAGE 26
NB CORE +1.1V	PAGE 27
NB RUN +1.1V	PAGE 28
DDR II SMD DR VTERM 1.8V(SUS)(TPS51116REGR)	PAGE 29
SYSTEM POWER ISL6237	PAGE 25
SYSTEM CHARGER (ISL6251A)	PAGE 24
DISCHARGER / +1.1V_S5, +1.2V,+2.5V	PAGE 30

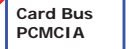
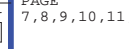
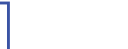
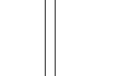
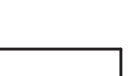
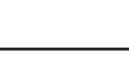
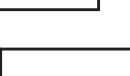
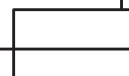
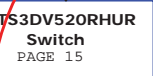
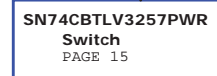


ZY5D NO USED

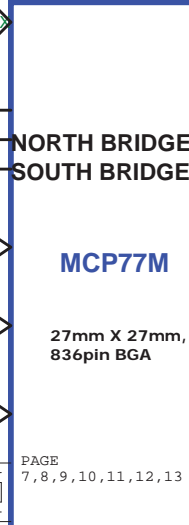


PCI-Express 16x

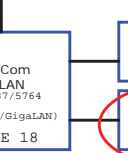
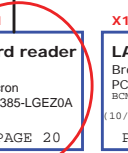
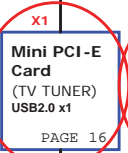
HT3 LINK



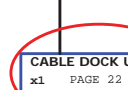
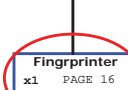
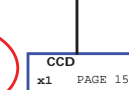
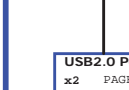
LAYER 1 : TOP
LAYER 2 : SGND1
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : GND



PCI-E

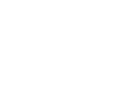
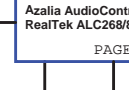
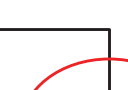
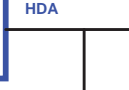


USB2.0



PCI

HDA





## PROCESSOR HYPERTRANSPORT INTERFACE

VLDLT\_Ax AND VLDLT\_Bx ARE CONNECTED TO THE LDT\_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

REV:B Modify

VLDLT\_RUN

U25A

HT LINK

VLDLT\_A0 VLDLT\_B0  
VLDLT\_A1 VLDLT\_B1  
VLDLT\_A2 VLDLT\_B2  
VLDLT\_A3 VLDLT\_B3

AE2 AE3  
AE4 AE5

C496

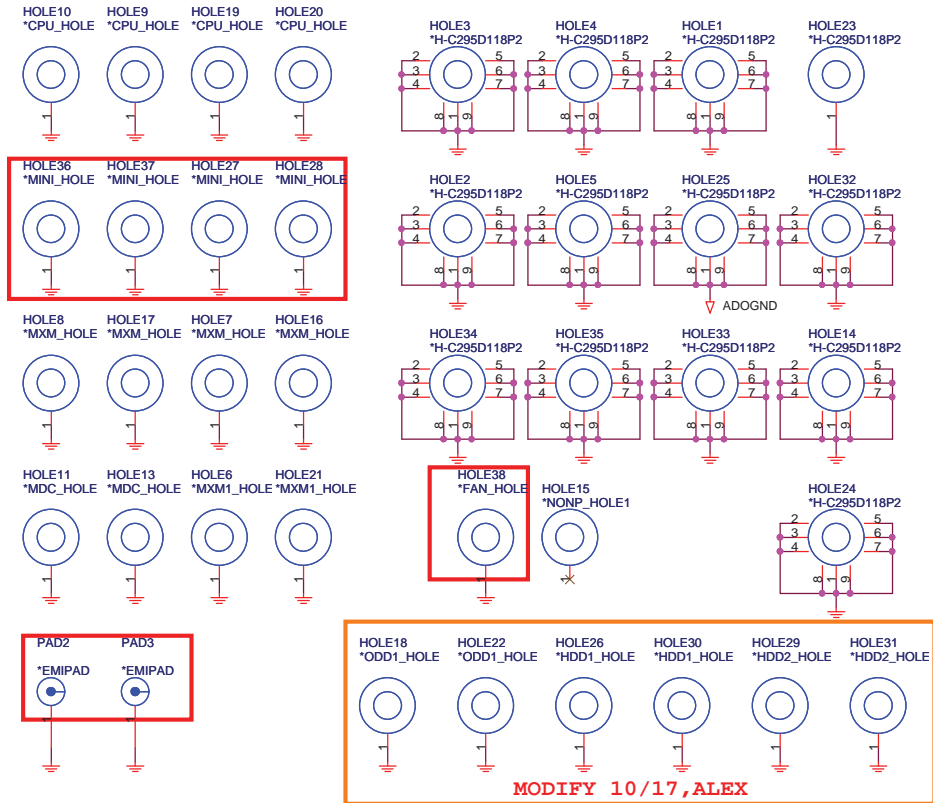
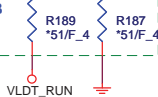
4.7u/6.3V\_6

HT_RXD0	E3	L0_CADIN_H0	AD1	HT_TXD0
HT_RXD1	E2	L0_CADIN_L0	AC1	HT_TXD1
HT_RXD2	E1	L0_CADIN_H1	AC2	HT_TXD2
HT_RXD3	G3	L0_CADIN_L1	AB1	HT_TXD3
HT_RXD4	G2	L0_CADIN_H2	AA1	HT_TXD4
HT_RXD5	G1	L0_CADIN_L2	AA2	HT_TXD5
HT_RXD6	H1	L0_CADIN_H3	AA3	HT_TXD6
HT_RXD7	J1	L0_CADIN_L3	W2	HT_TXD7
HT_RXD8	K1	L0_CADIN_H4	W3	HT_TXD8
HT_RXD9	L3	L0_CADIN_L4	V1	HT_TXD9
HT_RXD10	L2	L0_CADIN_H5	U1	HT_TXD10
HT_RXD11	L1	L0_CADIN_L5	U2	HT_TXD11
HT_RXD12	M1	L0_CADIN_H6	U3	HT_TXD12
HT_RXD13	N3	L0_CADIN_L6	T1	HT_TXD13
HT_RXD14	N2	L0_CADIN_H7	R1	HT_TXD14
HT_RXD15	E5	L0_CADIN_L7	AD4	HT_TXD15
HT_RXD16	F5	L0_CADIN_H8	AD3	HT_TXD16
HT_RXD17	F3	L0_CADIN_L8	AD5	HT_TXD17
HT_RXD18	F4	L0_CADIN_H9	ACS	HT_TXD18
HT_RXD19	G5	L0_CADIN_L9	AB3	HT_TXD19
HT_RXD20	H5	L0_CADIN_H10	AB4	HT_TXD20
HT_RXD21	H3	L0_CADIN_L10	AB5	HT_TXD21
HT_RXD22	H4	L0_CADIN_H11	AA5	HT_TXD22
HT_RXD23	K3	L0_CADIN_L11	Y5	HT_TXD23
HT_RXD24	K4	L0_CADIN_H12	W5	HT_TXD24
HT_RXD25	L5	L0_CADIN_L12	V4	HT_TXD25
HT_RXD26	M5	L0_CADIN_H13	V3	HT_TXD26
HT_RXD27	M3	L0_CADIN_L13	V5	HT_TXD27
HT_RXD28	M4	L0_CADIN_H14	U5	HT_TXD28
HT_RXD29	N5	L0_CADIN_L14	T4	HT_TXD29
HT_RXD30	P5	L0_CADIN_H15	T3	HT_TXD30

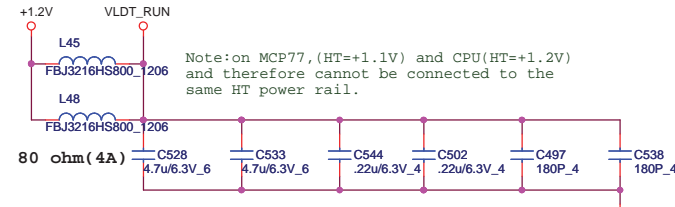
7 HT_CPU_UPCLK0	J3	L0_CLKIN_H0	Y1	HT_CPU_DWNCLK0	7
7 HT_CPU_UPCLK1	J2	L0_CLKIN_L0	W1	HT_CPU_DWNCLK1	7
7 HT_CPU_UPCLK2	J5	L0_CLKIN_H1	Y4	HT_CPU_DWNCLK2	7
7 HT_CPU_UPCLK3	K5	L0_CLKIN_L1	Y3	HT_CPU_DWNCLK3	7
7 HT_CPU_UPCTL0	N1	L0_CTLIN_H0	R2	HT_CPU_DWNCTL0	7
7 HT_CPU_UPCTL1	P1	L0_CTLIN_L0	R3	HT_CPU_DWNCTL1	7
7 HT_CPU_UPCTL2	P3	L0_CTLIN_H1	T5	HT_CPU_DWNCTL2	7
7 HT_CPU_UPCTL3	P4	L0_CTLIN_L1	R5	HT_CPU_DWNCTL3	7

Athlon 64 S1g2 SOCKET\_638\_PIN  
Athlon 64 S1g2  
Processor Socket  
SOCKET\_638\_PIN

NO STUB  
for HT3



MODIFY 10/17,ALEX



Note: on MCP77, (HT=+1.1V) and CPU(HT=+1.2V) and therefore cannot be connected to the same HT power rail.

**LAYOUT: Place bypass cap on topside of board**  
NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS  
PLACE CLOSE TO VLDLT0 POWER PINS



Quanta Computer Inc.

PROJECT : ZY5D

Size	Document Number	Rev
	AMD Griffin HT I/F	3B

Date: Wednesday, May 21, 2008 Sheet 2 of 35

### To reverse SODIMM socket

To normal SODIMM socket

Athlon 64 S1g2 SOCKET\_638\_PIN

M\_B\_DQS0  
M\_B\_DQS1  
M\_B\_DQS2  
M\_B\_DQS3  
M\_B\_DQS4  
M\_B\_DQS5  
M\_B\_DQS6  
M\_B\_DQS7

M\_A\_DQS0  
M\_A\_DQS1  
M\_A\_DQS2  
M\_A\_DQS3  
M\_A\_DQS4  
M\_A\_DQS5  
M\_A\_DQS6  
M\_A\_DQS7

6 M\_B\_DQS[0..7]

6 M\_A\_DQS[0..7] 6

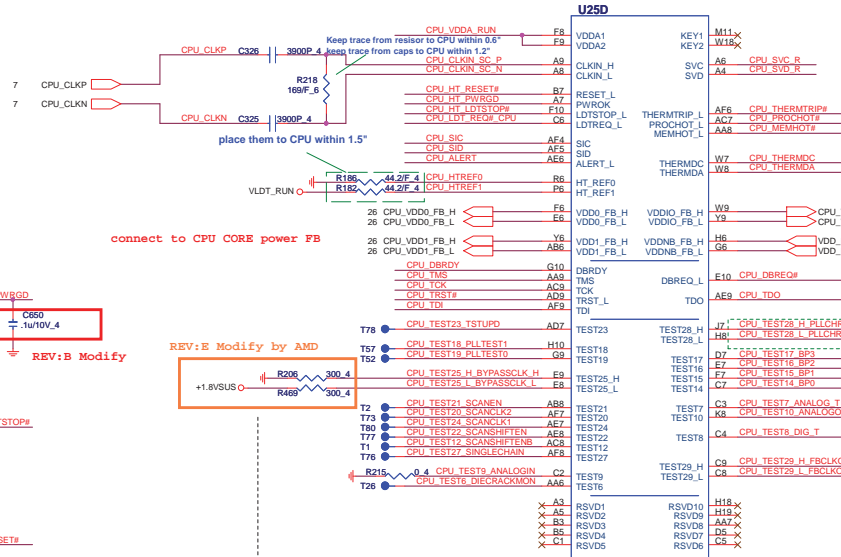
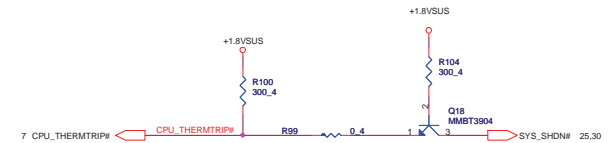
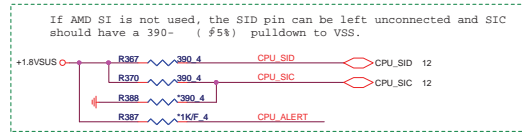
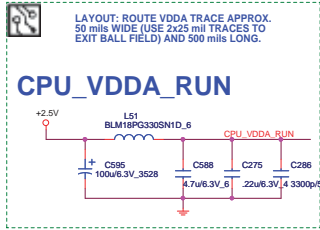
M\_B\_DQS#0  
M\_B\_DQS#1  
M\_B\_DQS#2  
M\_B\_DQS#3  
M\_B\_DQS#4  
M\_B\_DQS#5  
M\_B\_DQS#6  
M\_B\_DQS#7

M\_A\_DQS#0  
M\_A\_DQS#1  
M\_A\_DQS#2  
M\_A\_DQS#3  
M\_A\_DQS#4  
M\_A\_DQS#5  
M\_A\_DQS#6  
M\_A\_DQS#7

6 M\_B\_DQS#0..7]

6 M\_A\_DQS#0..7] 6

# ATHLON Control and Debug



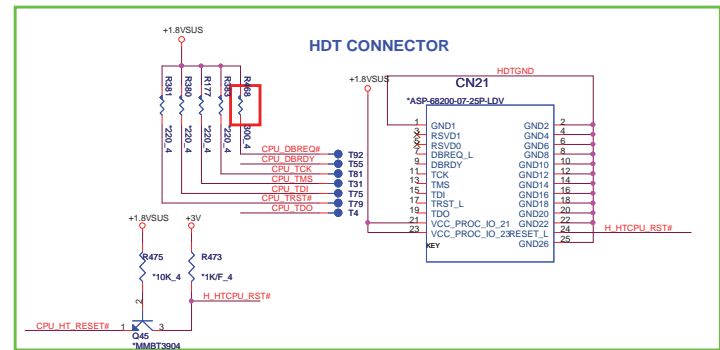
connect to CPU VDDIO power FB

connect to CPU VDDNB power FB

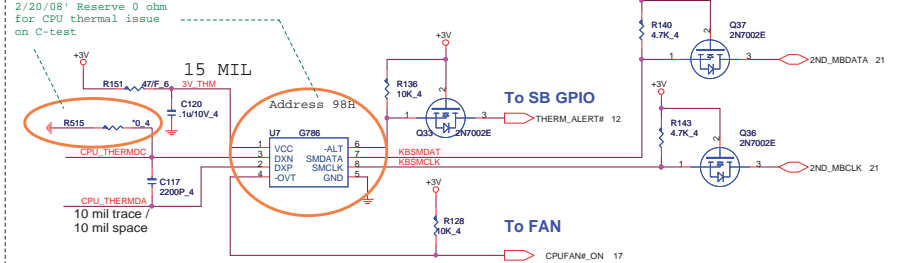
connect to CPU CORE power controller

VFIX MODE

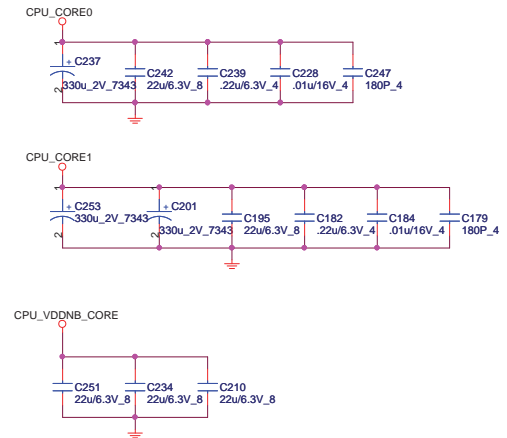
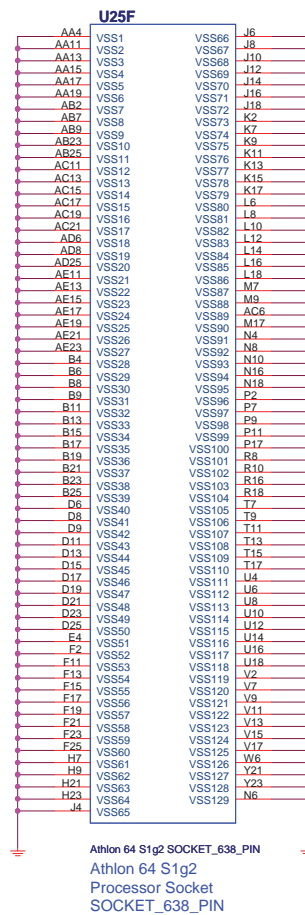
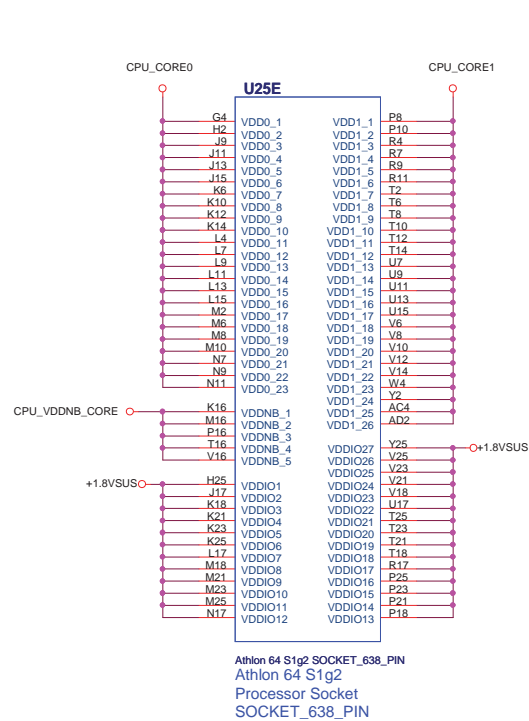
SVC	SVD	Voltage Output(CPU Power)
0	0	1.4V
0	1	1.2V
1	0	1.0V
1	1	0.8V



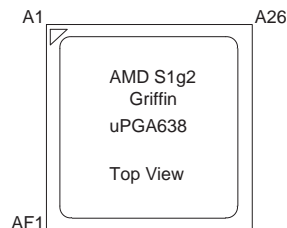
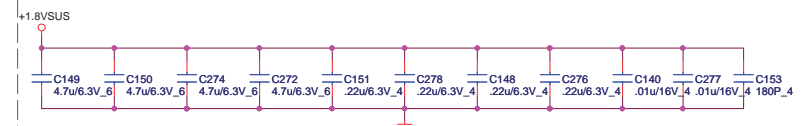
## CPU H/W MONITOR



## PROCESSOR POWER AND GROUND

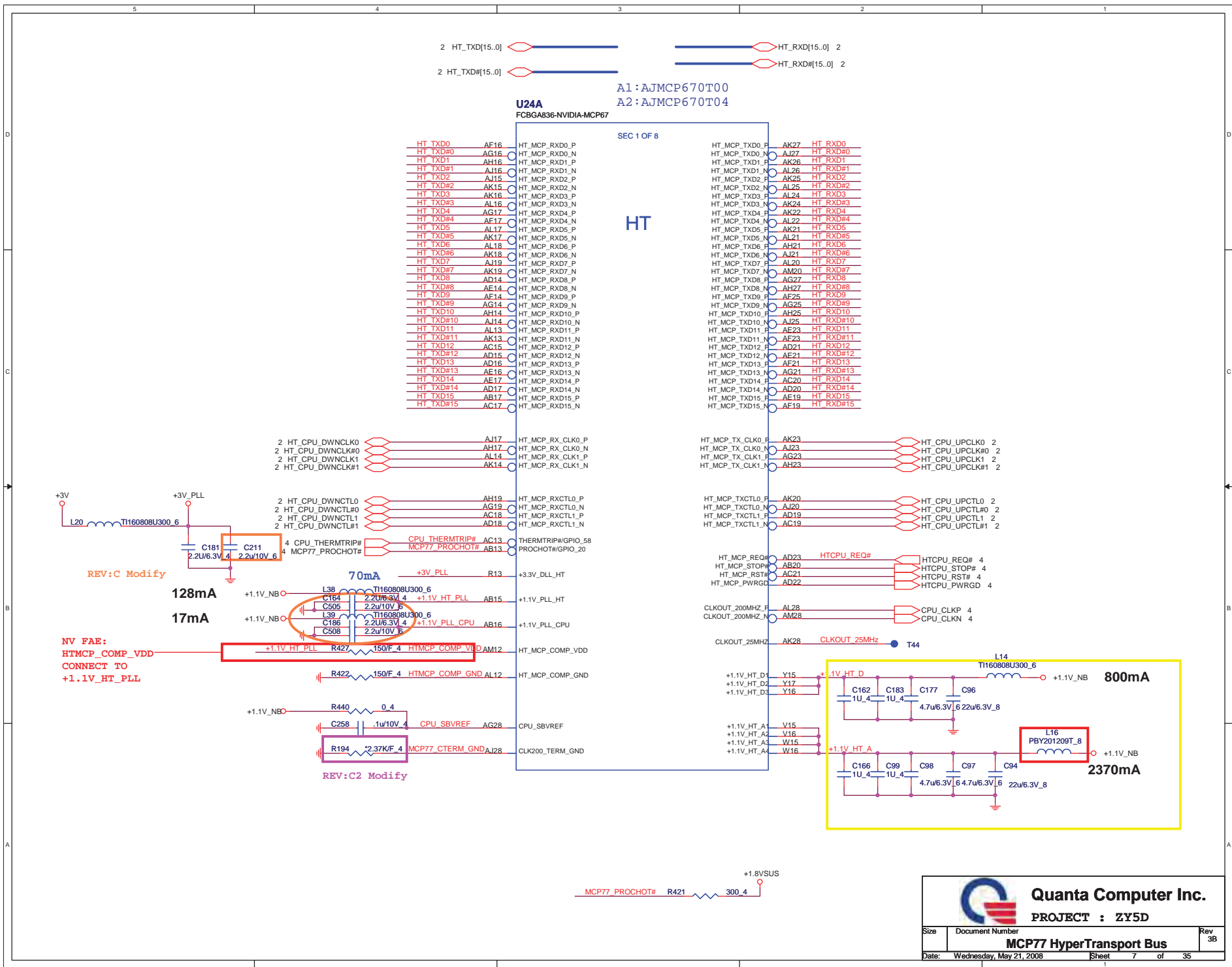


**DECOUPLING BETWEEN PROCESSOR AND DIMMs**  
**PLACE CLOSE TO PROCESSOR AS POSSIBLE**















**U24C**  
FCBGA36-NVIDIA-MCP67

SEC 3 OF 8

**LAN**

**DACS**

**FLAT  
PANEL**

**Notice**

PAGE : 10  
HDMI circuit  
ZY5D no use it

**Notice**

PAGE : 10  
HDMI circuit  
ZY5D no use it

[SATA HDD 1]

[SATA HDD 2]

[SATA ODD]

U24E  
FCBG836-NVIDIA-MCP67

SEC 5 OF 8

SATA

USB

REV:B Modify

MINI CARD \* 2

MINI CARD \* 2

BLUETOOTH

USB PULL-DOWN

REV:C Modify

INT LEFT USB 2

CARD READER

INT LEFT USB 1

Fingerprint

EXT USB \* 2

Docking

CCD

EXT USB \* 2

NEW CARD

REV:B Swap  
Modify

REV:C Modify

845 Ohm for MCP77 checklist

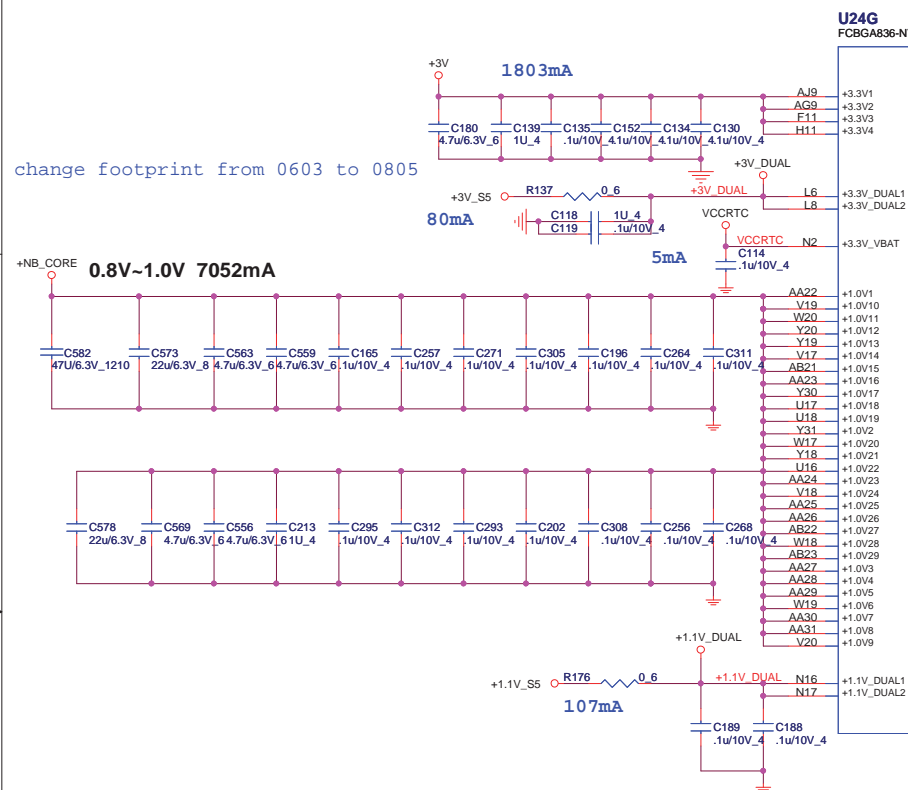


Quanta Computer Inc.  
PROJECT : ZY5D

Size	Document Number	Rev
	MCP77 SATA and USB	3B
Date:	Wednesday, May 21, 2008	Sheet 11 of 35



## MCP77 POWER PLANE/GND & BYPASS



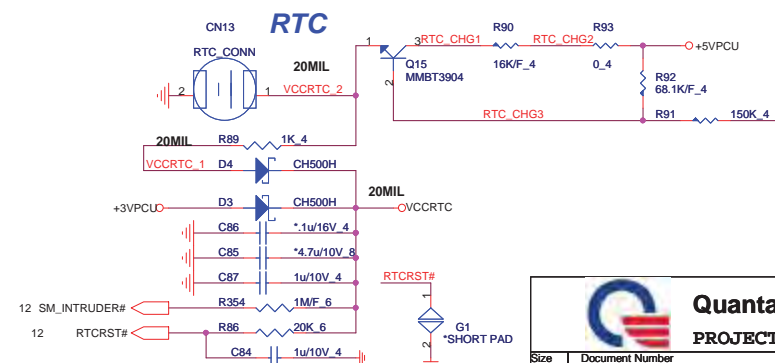
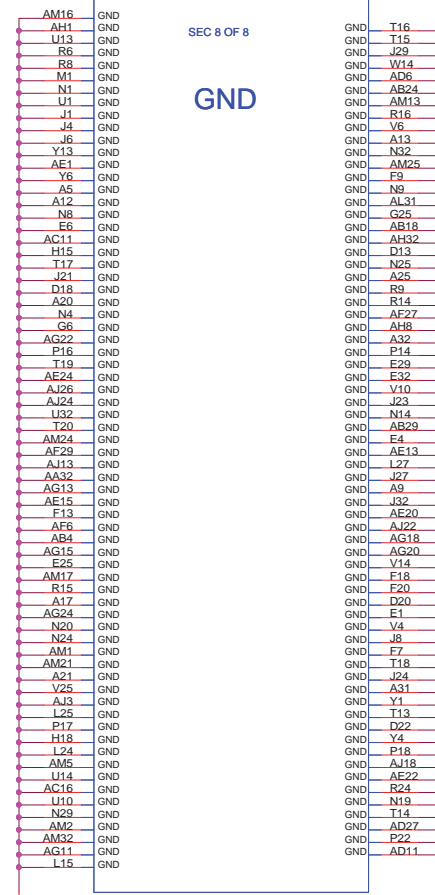
SEC 7 OF 8

PWR/GND



SEC 8 OF 8

GND

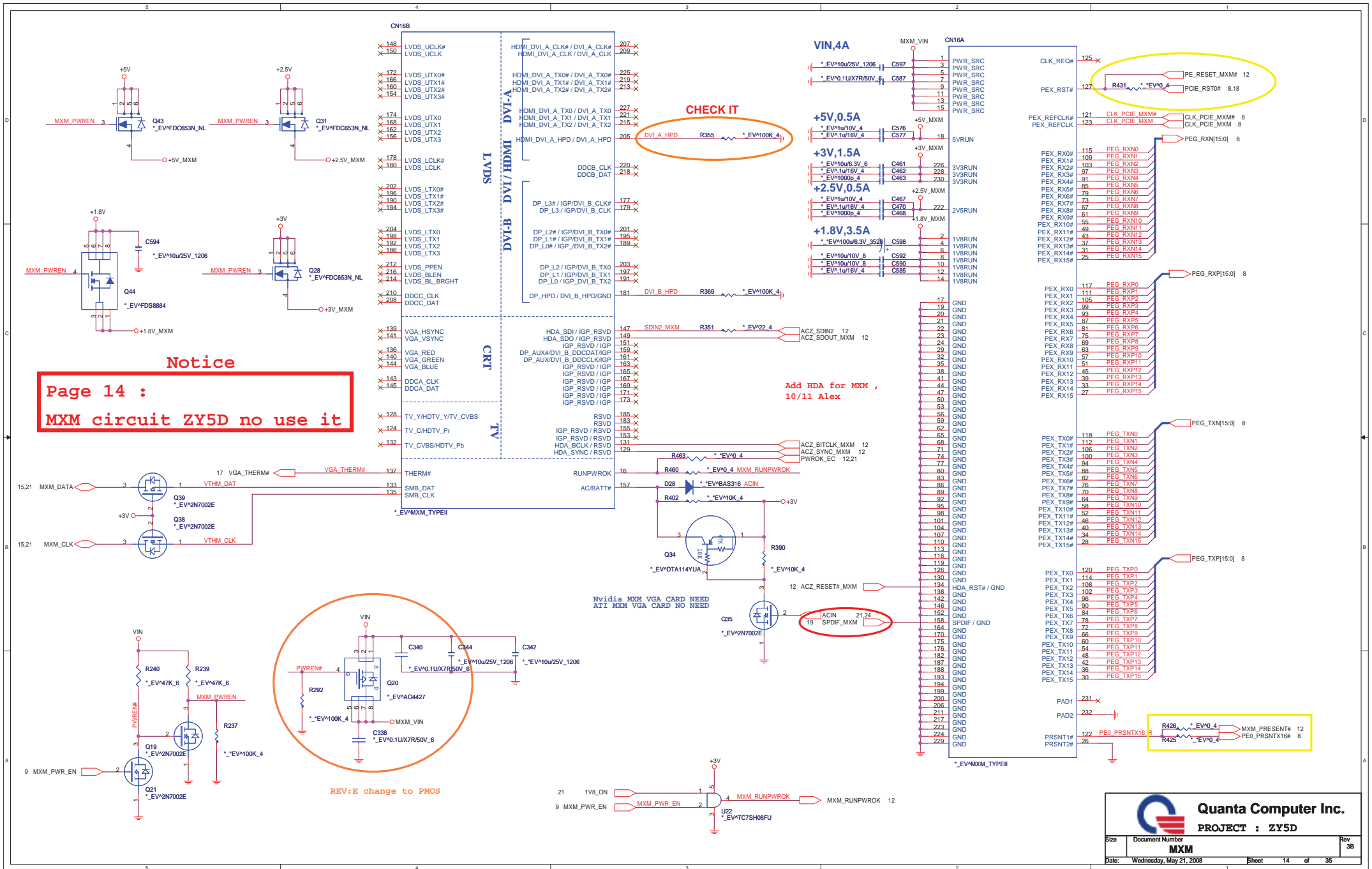


**Quanta Computer Inc.**  
**PROJECT : ZY5D**

Size	Document Number	Rev
	<b>MCP77 POWER/GND</b>	<b>3B</b>
Date:	Wednesday, May 21, 2008	Sheet 13 of 35

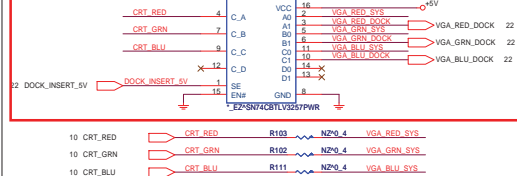
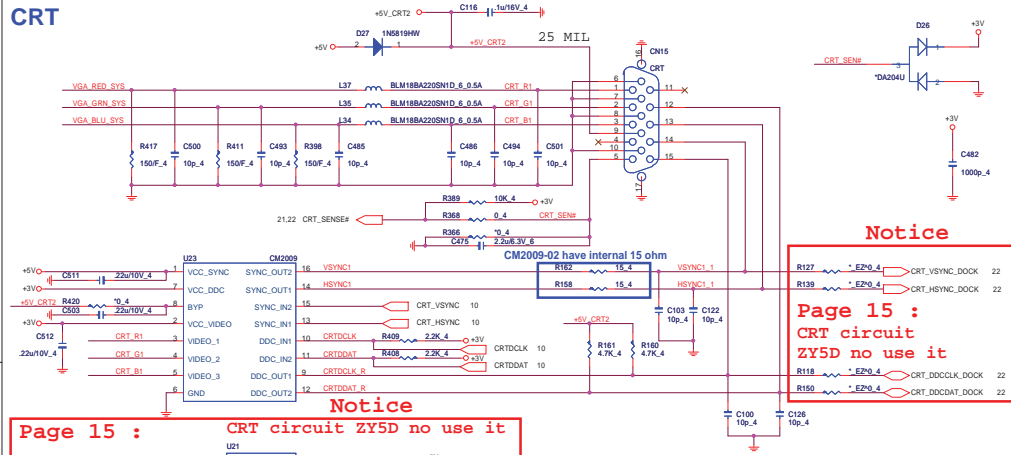
# Notice

Page 14 :  
MXM circuit ZY5D no use it

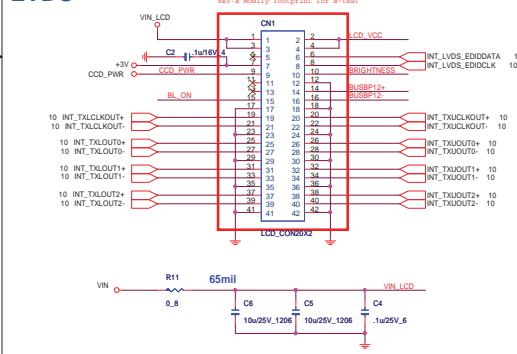




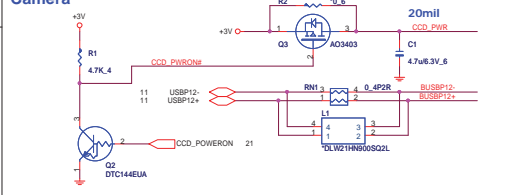
# CRT



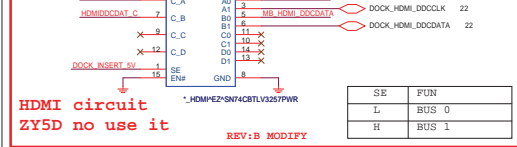
# LVDS



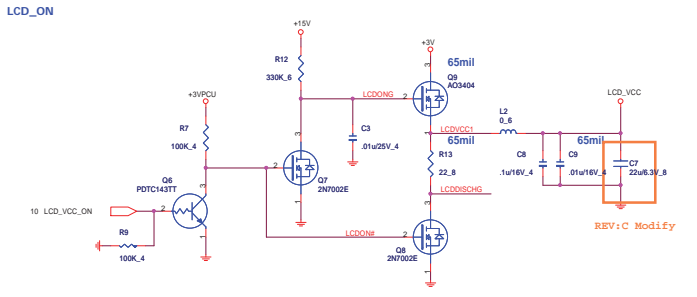
# Camera



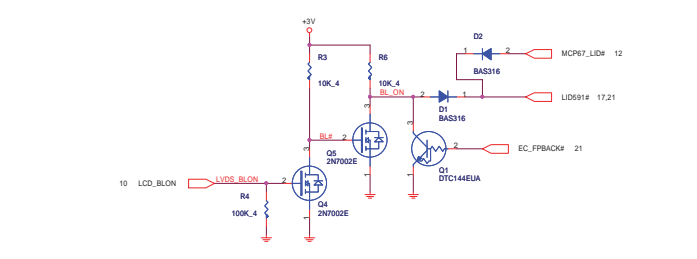
# HDMI



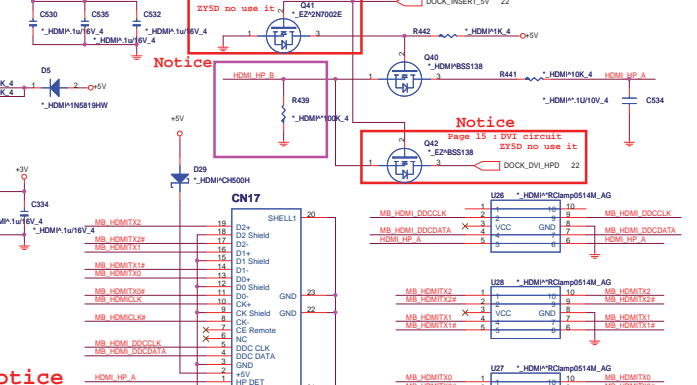
# LCD\_ON



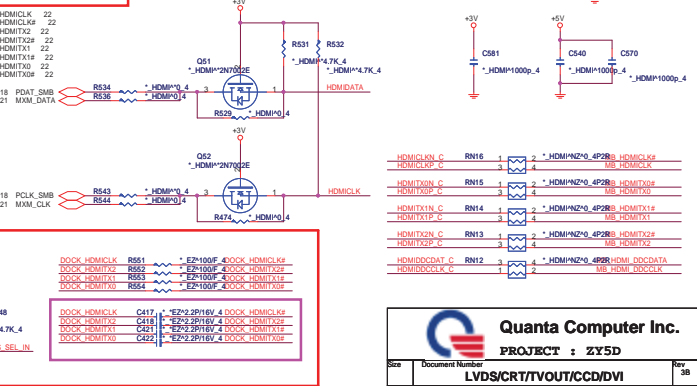
# Backlight Control



# HDMI

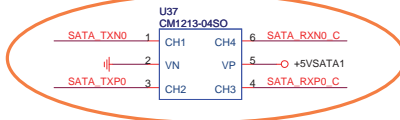


# HDMI

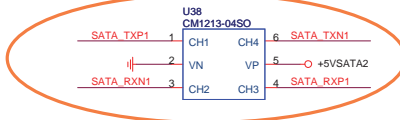




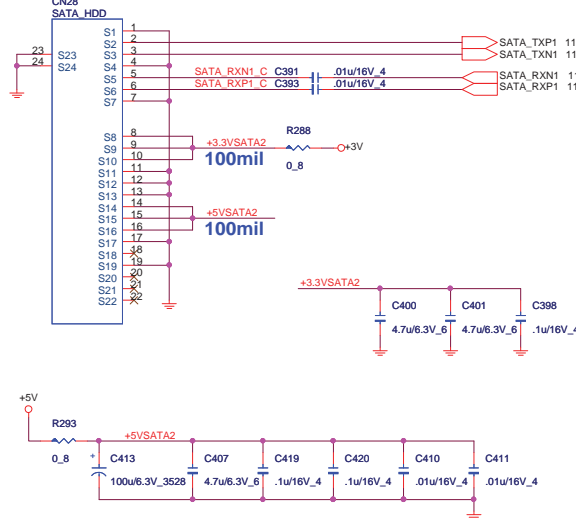
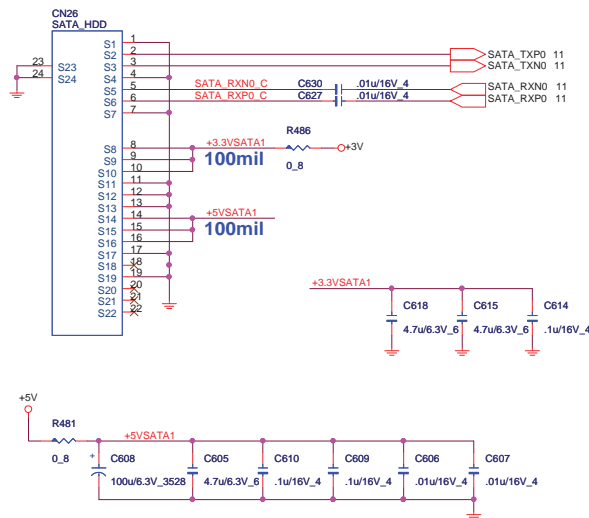
## SATA1



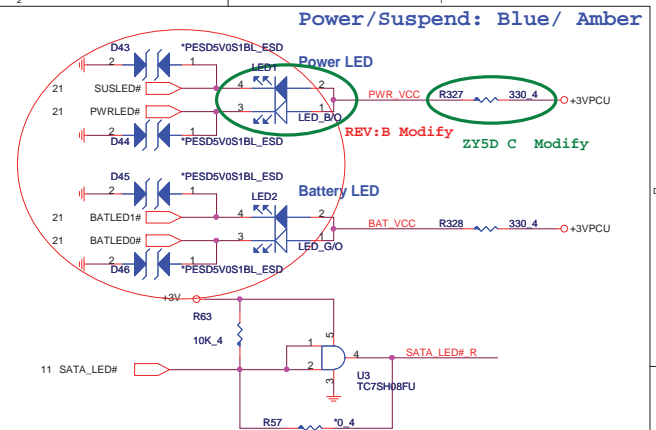
## SATA2



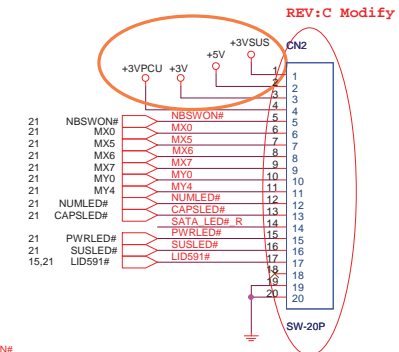
REV:E add ESD



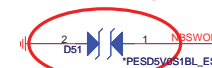
## LED



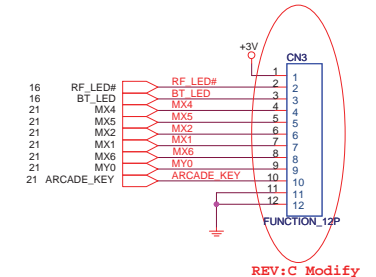
## To Power/B



REV:B Modify

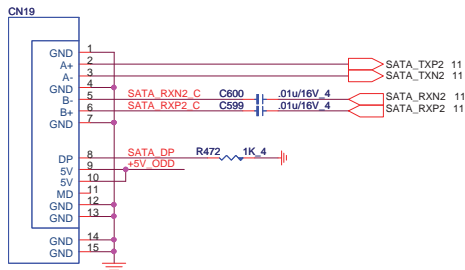


## To Switch/B

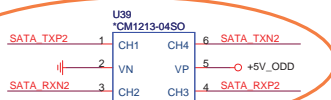
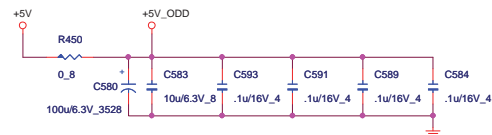


REV:C Modify

## ODD (SATA)

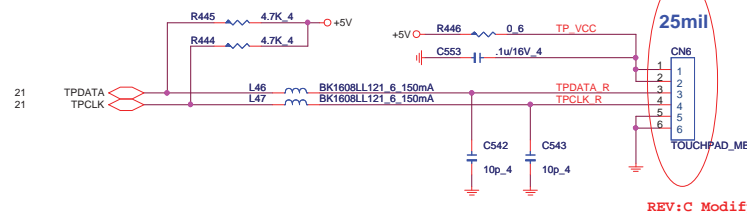


C16654-122A4-L\_Serial\_ATA



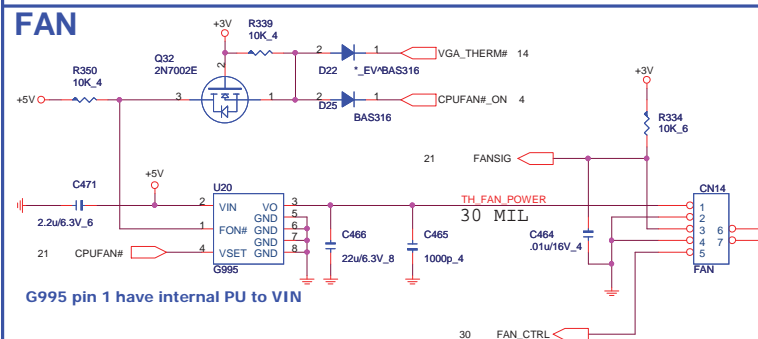
REV:E add ESD

## TP CONN



REV:C Modify

## FAN

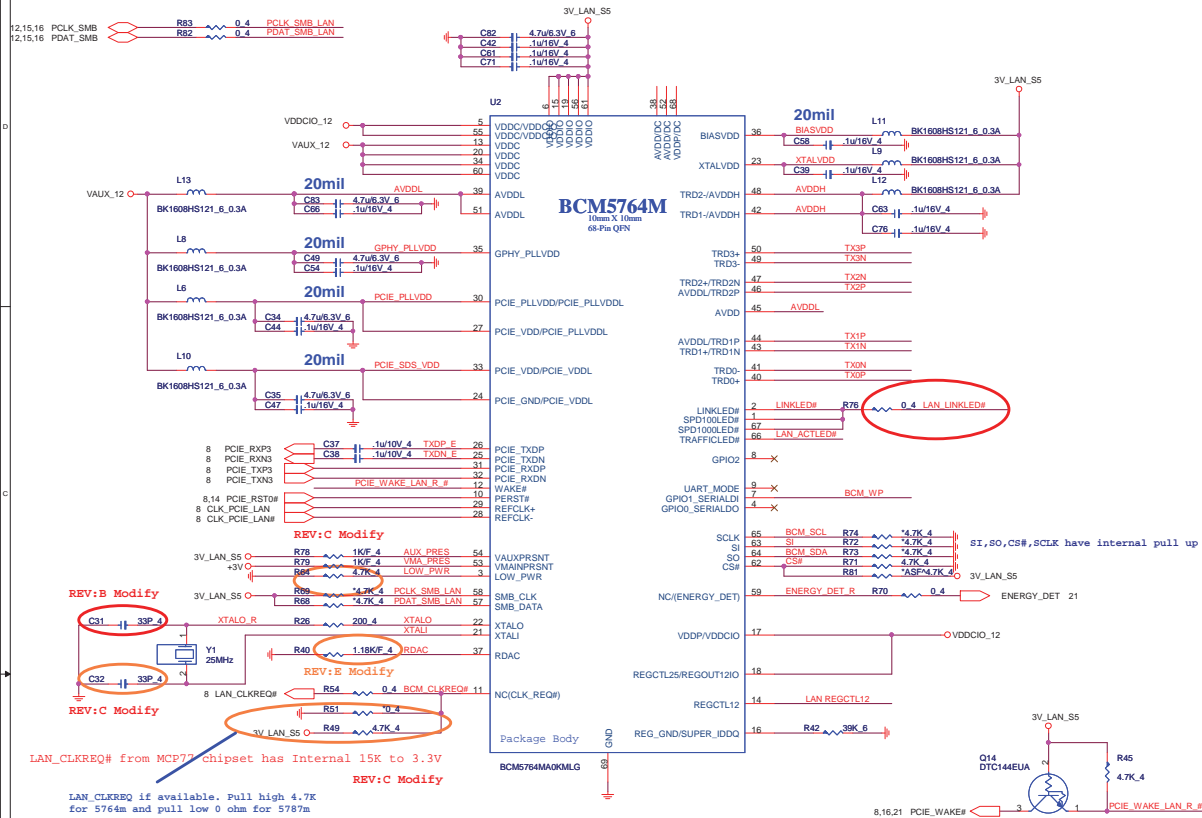


G995 pin 1 have internal PU to VIN

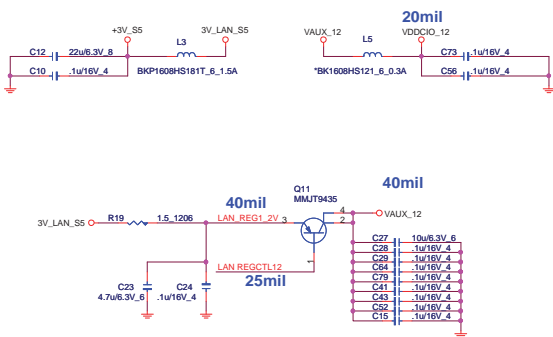


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PROJECT : ZY5D

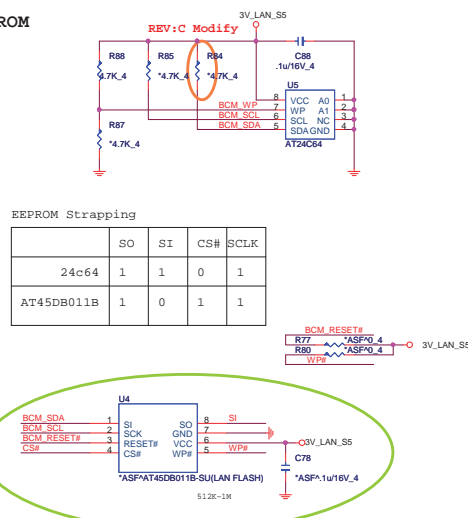
## Giga LAN BCM5787M/5764M



## LAN POWER

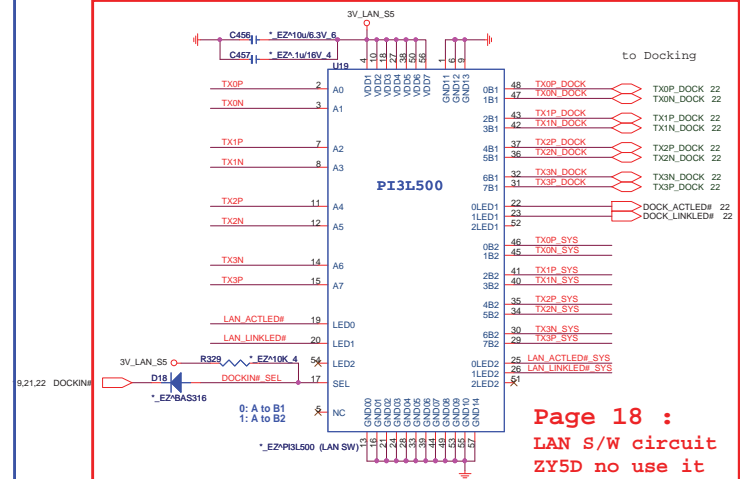


## EEPROM



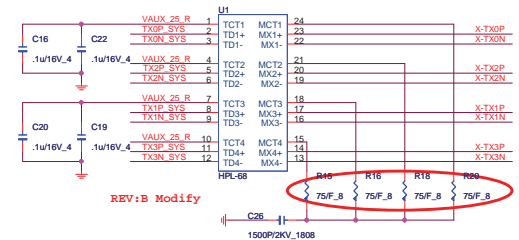
## LAN SWITCH

## Notice

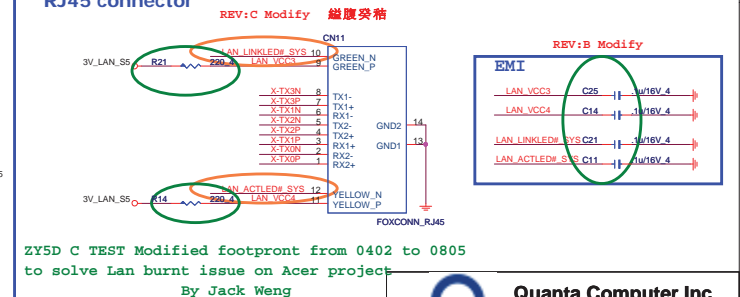


## Transformer

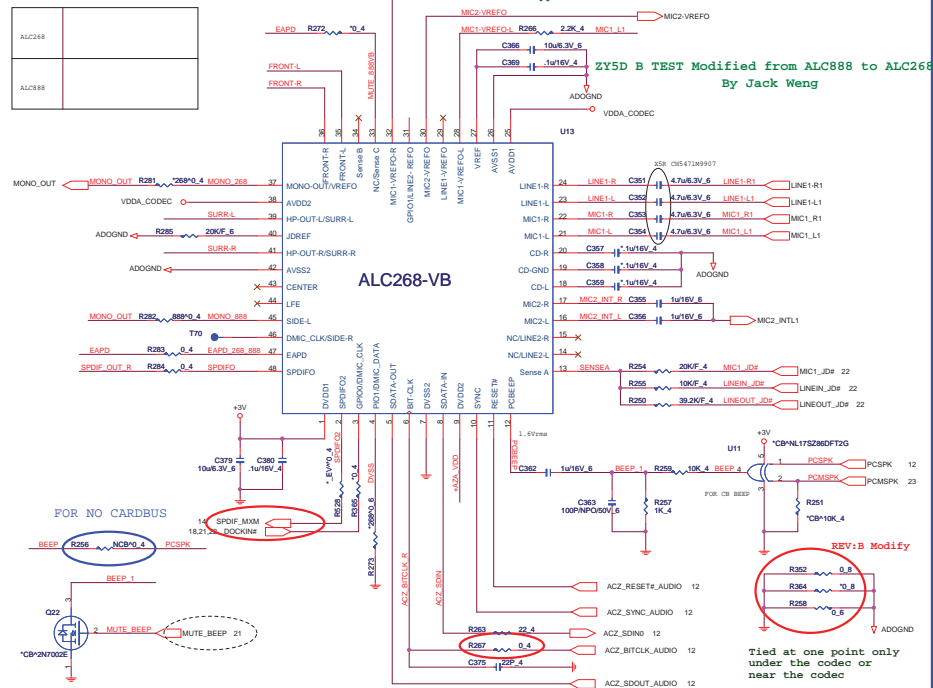
Source 1: DELTA LFE9249 DB0Z1LAN11  
Source 2: Bothand GST5009 DBKN1NLAN03



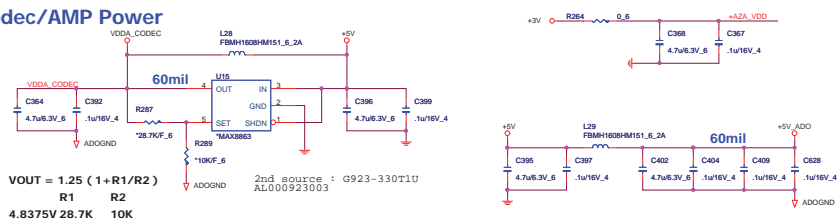
## RJ45 connector



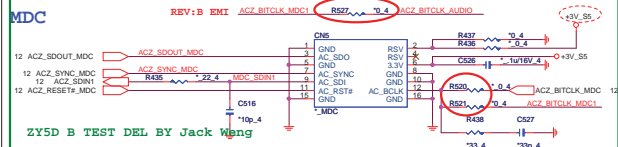
## CODEC



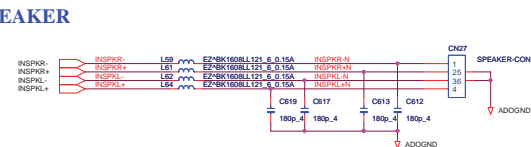
### Codec/AMP Power



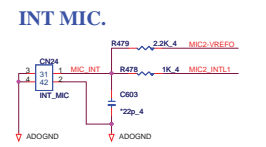
## MDC



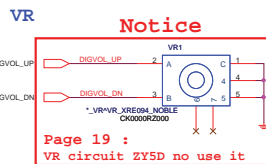
**SPEAKER**



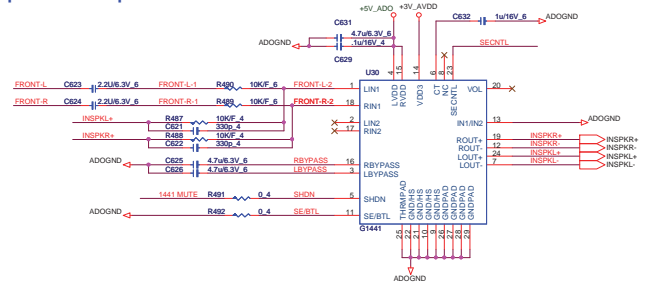
**INT MIC.**



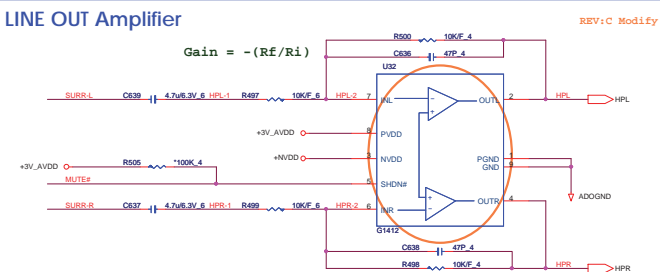
## VR



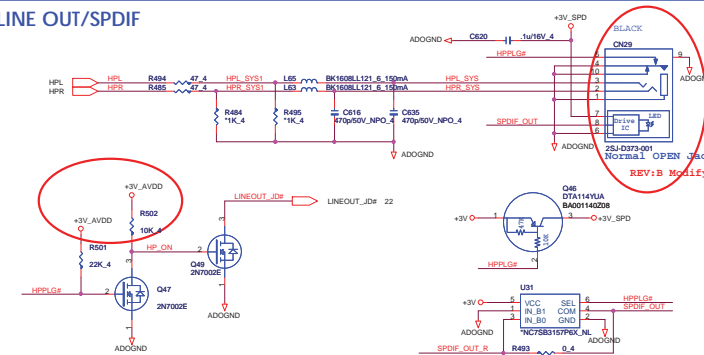
## Speaker Amplifier



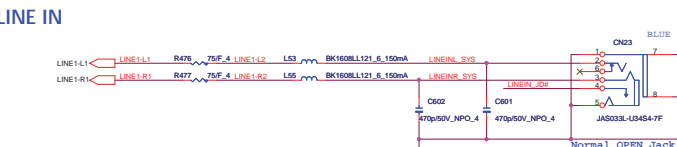
## LINE OUT Amplifier



LINE OUT/SPDIF



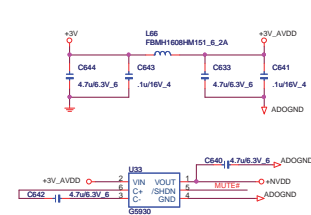
## LINE IN



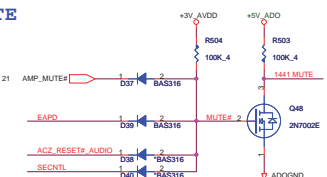
## MIC



## Amplifier POWER

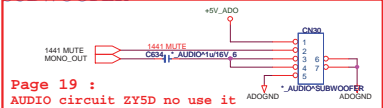


## MUTE



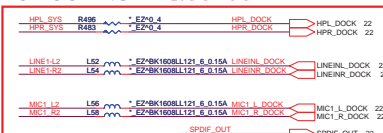
**SUBWOOFER**

## Notice



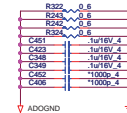
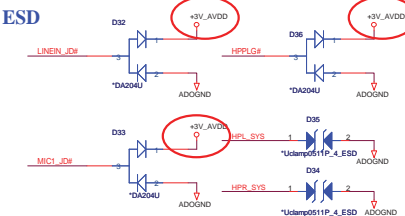
## TO DOCKING

## Notice



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AUDIO circuit ZY5D no use it

**ESD**











## NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME. IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS. THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

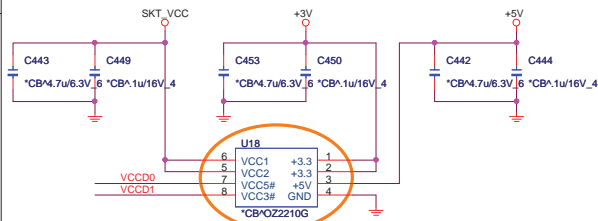
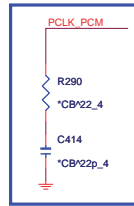
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP\_PGM TO CREATE VPP\_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127

AD20 R309 \*CB\*100F\_4 PCM IDSEL

ID Select : AD20  
Interrupt Pin : INTA#  
Request Indicate : REQ0#  
Grant Indicate : GNT0#

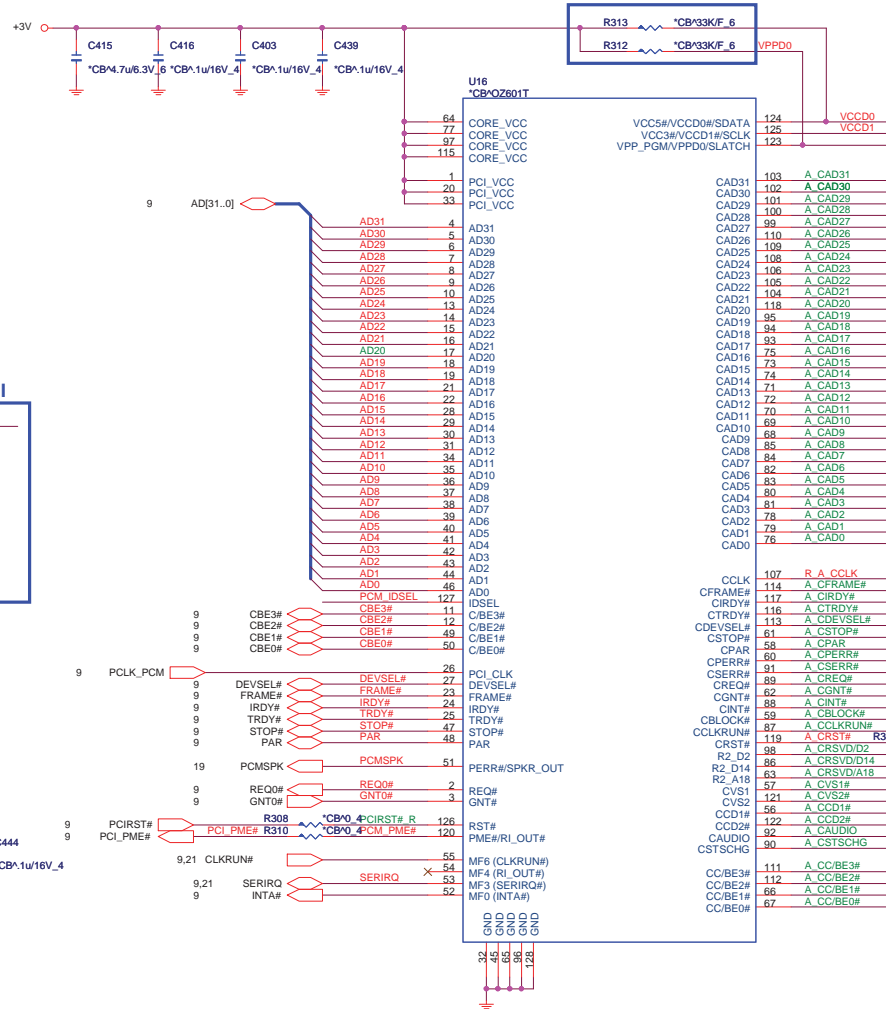
For EMI



Check Footprint & P/N

22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.

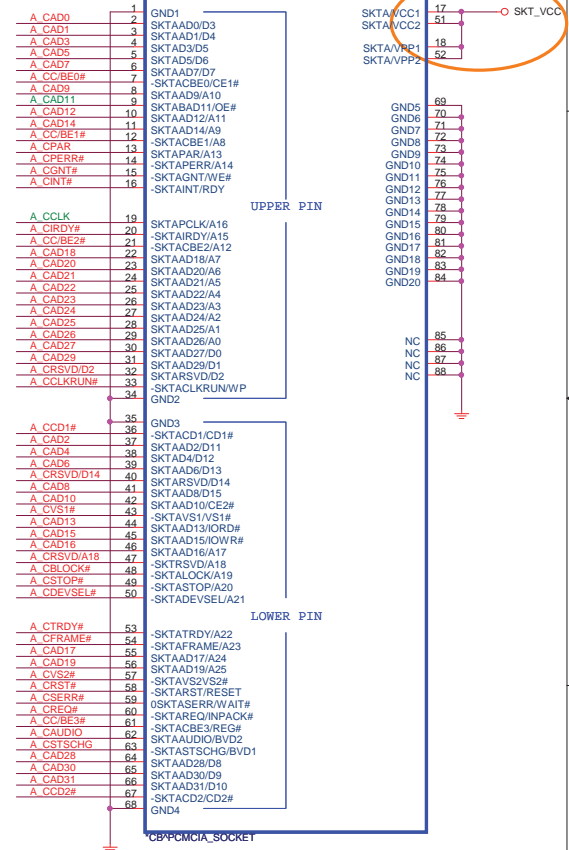
IDSEL SELECT POWER-ON-STRAPPING  
(SEE NOTE & TABLE FOR OPTIONS)



R A CCLK R307 \*CB\*33K\_F\_4 A CCLK

PCMCIA SOCKET

Check it

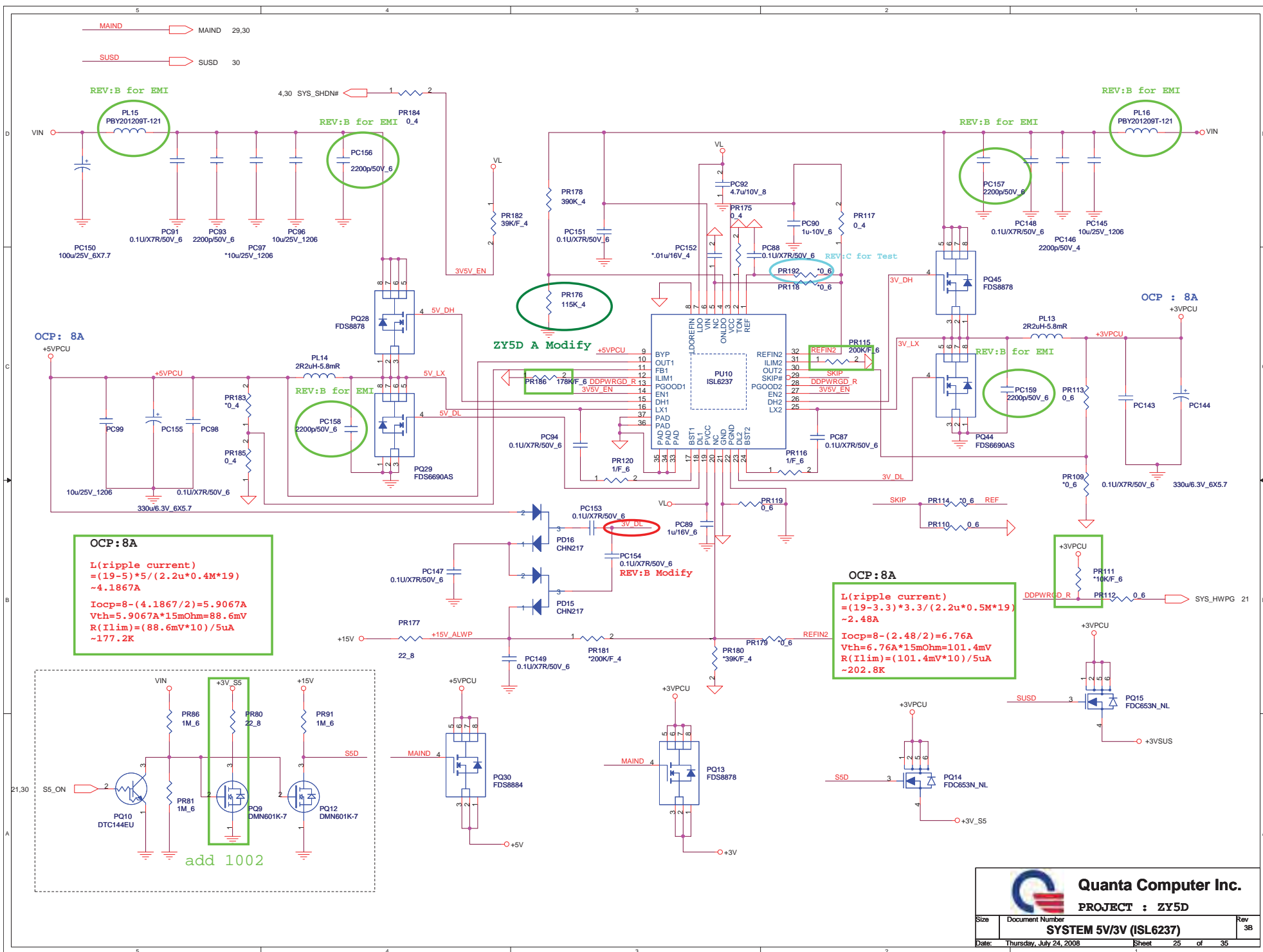


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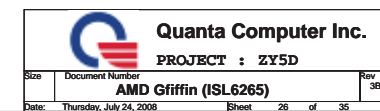
PROJECT : ZY5D

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	PCMCIA(OZ601)	3B
Date:	Wednesday, May 21, 2008	Sheet 23 of 35

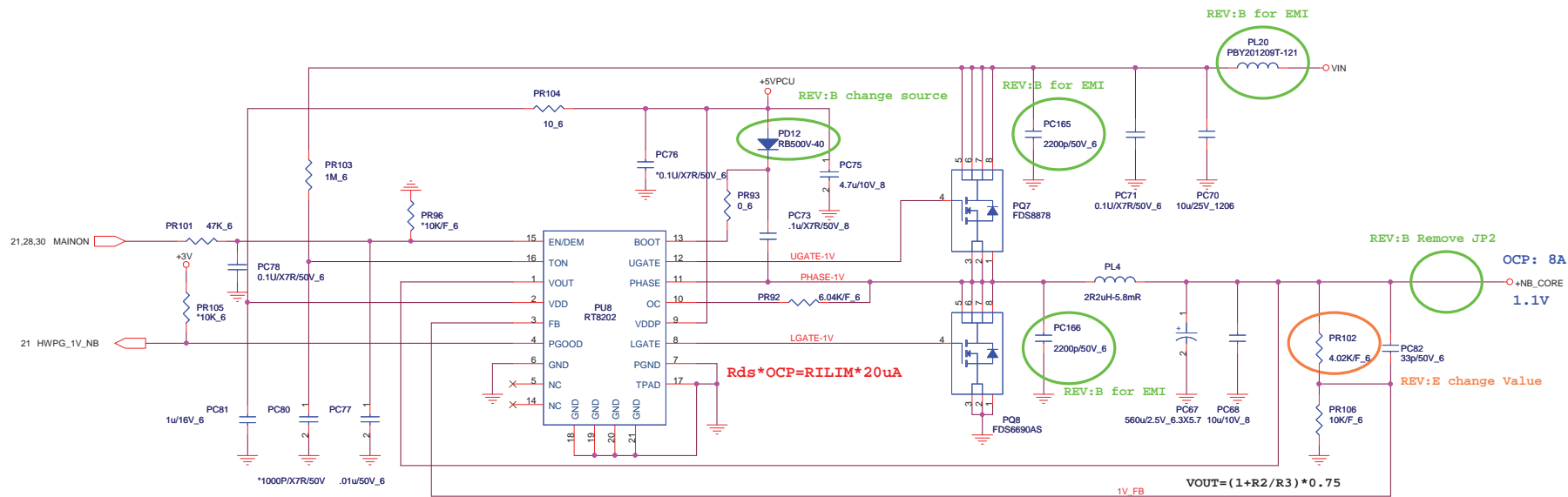


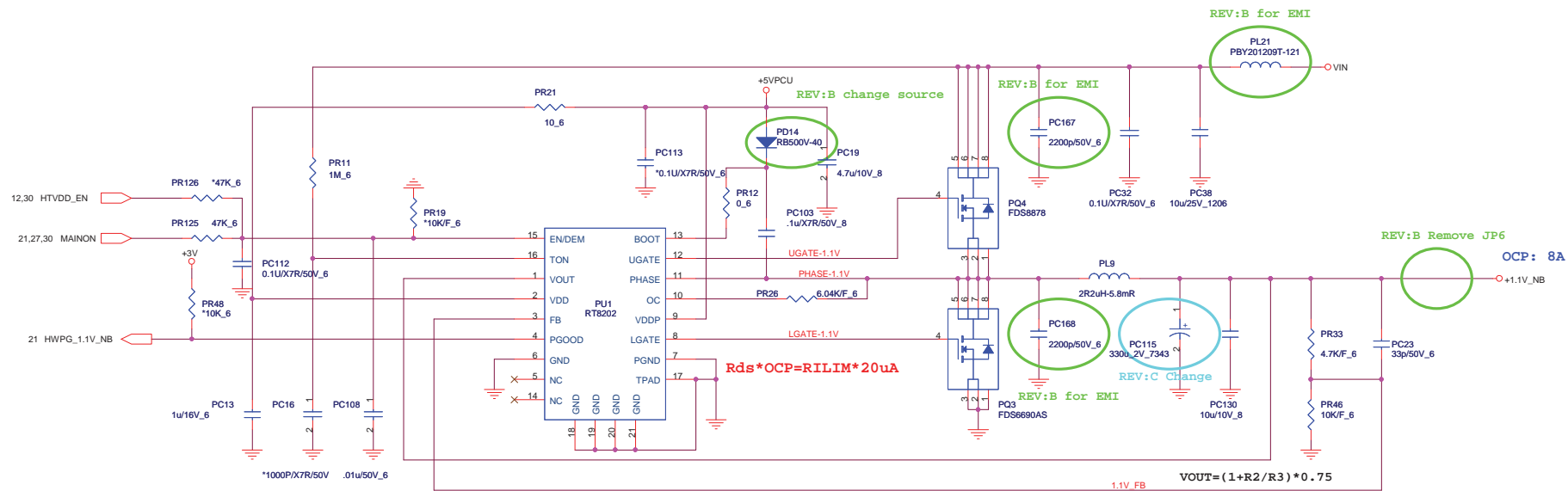


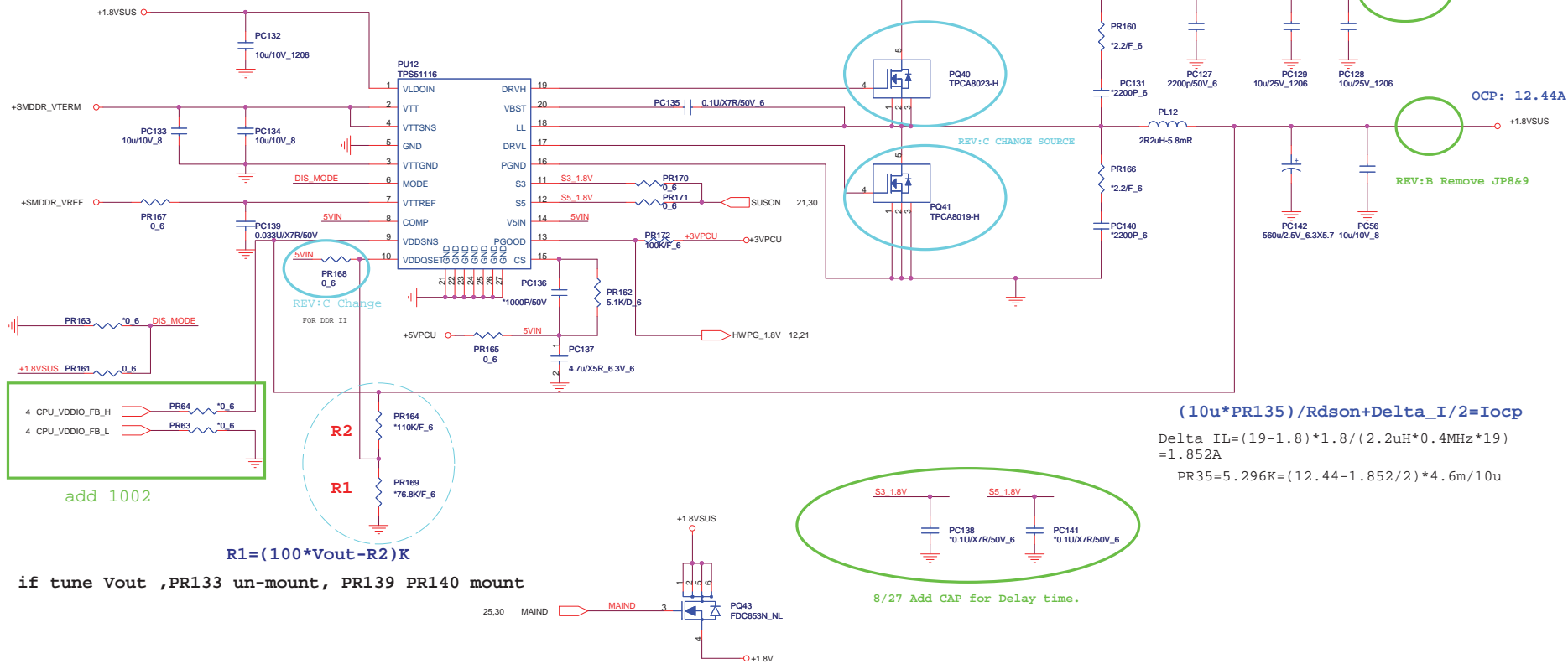
SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8









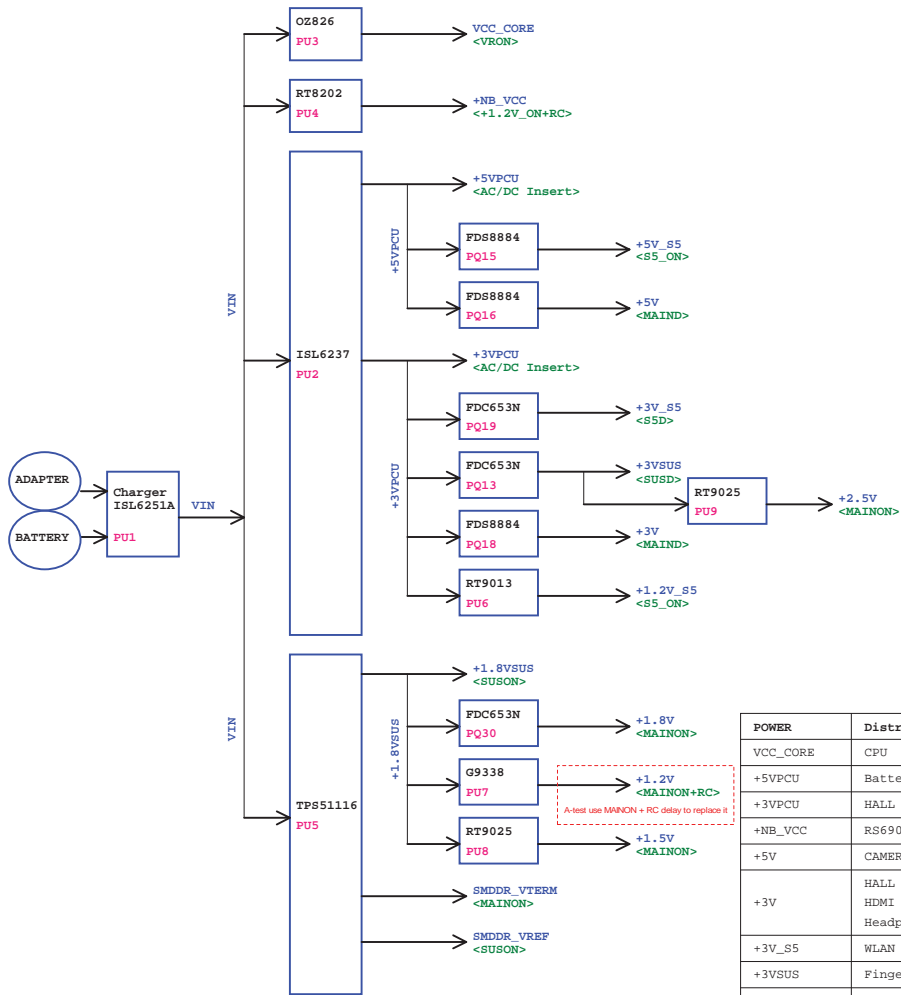


$$(10u \cdot PR135) / R_{dson} + \Delta I / 2 = I_{ocp}$$

$$\Delta I_L = (19 - 1.8) \cdot 1.8 / (2.2uH \cdot 0.4MHz \cdot 19) = 1.852A$$

$$PR35 = 5.296K = (12.44 - 1.852 / 2) \cdot 4.6m / 10u$$





POWER	Distribution
VCC_CORE	CPU
+5VPCU	Battery LED , Power LED , USB , CIR , RTC
+3VPCU	HALL SENSOR , Battery LED , RF LED , kill SW , Jumper LED , KB , Power Board , EC , ID , SPI Flash , CIR
+NB_VCC	RS690M
+5V	CAMERA , Card Reader LED , ODD/HDD LED , Felica , T/P , T/sensor , CRT , HDMI , SB600 , CPU FAN , MXM , Headphone , EC , INT SPK AMP
+3V	HALL SENSOR , LCD PANEL , LVDS , WLAN , HD Decoder , NEW CARD , KB , KB LED , XD LED , Blue tooth , Touch sensor , Card Reader (OZ129) , ODD/HDD , HDMI , CRT , TVOUT , REQUIRED STRAPS , DEBUG STRAPS , SB600 , RS690M , DDR , CPU Thermal monitor , CPU FAN , CLK , MXM , VR , FM Tuner MDC , Headphone , EC , LAN , Codec(CX 20561)
+3V_S5	WLAN , NEW CARD , SB600 , MXM , LAN
+3VSUS	Finger print , SB600
+2.5V	CPU
+1.2V_S5	SB600
+1.8VSUS	SB600 , DDR , CPU , HDT
+1.8V	SB600 , LCD , LVDS , RS690M
+1.2V	SB600 , RS690M , CPU , WLAN , HD Decoder , NEW CARD
+SMDDR_VTERM	DDR , CPU
+SMDDR_VREF	DDR
+5V_S5	

# ZY5 Power on Sequence

